

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a plurality of regions;

5 a resistor group including a plurality of resistors provided in one of said regions of said semiconductor substrate;

a metal interconnection layer above the region in which said resistor group has been provided; and

10 a shielding layer between said resistor group and said metal interconnection layer.

2. The semiconductor device according to claim 1, comprising at least a DRAM region and a logic region,

15 wherein a layer common to a bit line layer in said DRAM region is used as a shielding layer in said logic region.

3. The semiconductor device according to claim 1,

comprising at least a DRAM region with a stacked capacitor

20 and a logic region, wherein said stacked capacitor in said DRAM region is composed of a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

25 a layer common to said upper capacitor electrode layer in said DRAM region is used as a shielding layer in said

logic region.

4. The semiconductor device according to claim 1, wherein
a potential of said shielding layer is fixed.

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5. A semiconductor device comprising:
a semiconductor substrate;
a signal interconnection layer on said semiconductor
substrate; and

10 a shielding layer on one side of said signal
interconnection layer, or shielding layers on both sides
of said signal interconnection layer.

15 6. The semiconductor device according to claim 5,
comprising at least a DRAM region and a logic region,
wherein a layer common to a gate electrode layer in
said DRAM region is used as a shielding layer in said logic
region.

20 7. The semiconductor device according to claim 5,
comprising at least a DRAM region and a logic region,
wherein a layer common to a bit line layer in said
DRAM region is used as a shielding layer in said logic region.

8. The semiconductor device according to claim 5, comprising at least a DRAM region with a stacked capacitor and a logic region, wherein said stacked capacitor in said DRAM region is composed of a lower capacitor electrode 5 layer, a dielectric film, and an upper capacitor electrode layer, and

Sub A10
a layer common to said upper capacitor electrode layer in said DRAM region is used as a shielding layer in said logic region.

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9. The semiconductor device according to claim 5, wherein a potential of said shielding layer is fixed.

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10. A method of fabricating a semiconductor device having at least a DRAM region and a logic region and having a resistor group in said logic region, the method comprising:

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forming a resistor group in said logic region;
forming a shielding layer in said DRAM region and said logic region; and
forming a metal interconnection layer above a portion of said logic region in which said resistor group has been formed.

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11. The method according to claim 10, wherein said shielding layer is a bit line layer.

12. The method according to claim 10, further comprising
5 forming a stacked capacitor composed of a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region,

SCW
wherein said capacitor electrode layer is used as said shielding layer.

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13. The method according to claim 10, further comprising fixing a potential of said shielding layer.

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14. A method of fabricating a semiconductor device having at least a DRAM region and a logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a signal interconnection layer in said logic region; and

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forming a shielding layer on one side of said signal interconnection layer, or forming shielding layers on both sides of said signal interconnection layer, in said DRAM region and said logic region.

Sub B1
15. The method according to claim 14, wherein said shielding layer is a gate electrode layer.

16. The method according to claim 14, wherein said 5 shielding layer is a bit line layer.

Sub C12
17. The method according to claim 14, further comprising forming a stacked capacitor composed of a lower capacitor electrode layer, a dielectric film, and an upper capacitor 10 electrode layer in said DRAM region,

wherein said capacitor electrode layer is used as said shielding layer.

18. The method according to claim 14, further comprising 15 fixing a potential of said shielding layer.

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